Fig. 1A

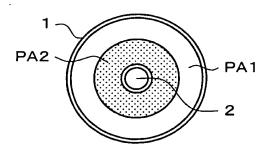


Fig. 1B

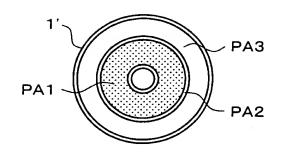
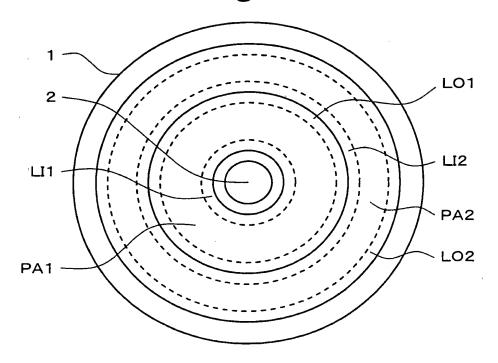


Fig. 2



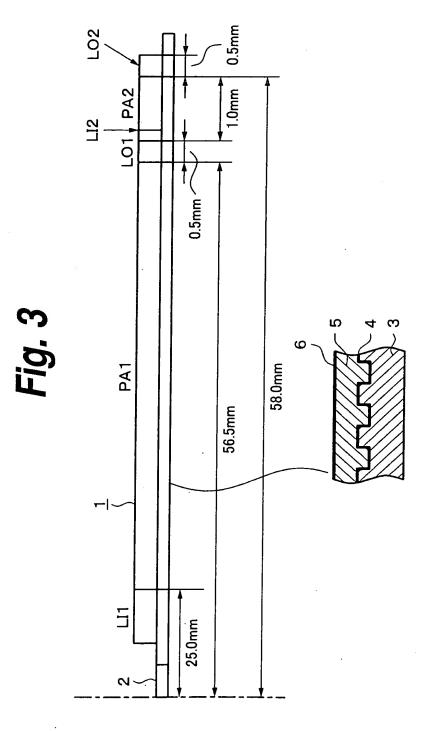
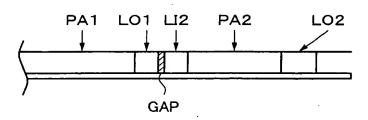
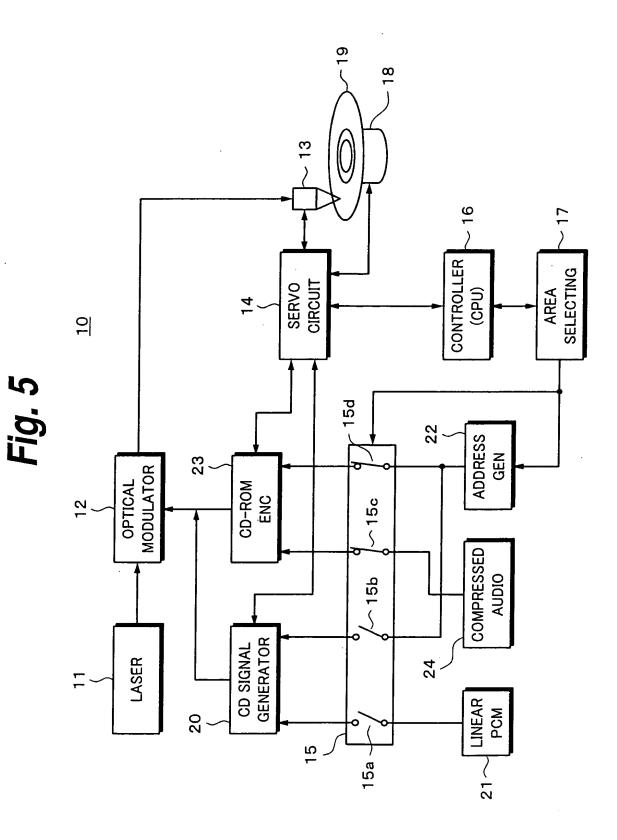


Fig. 4





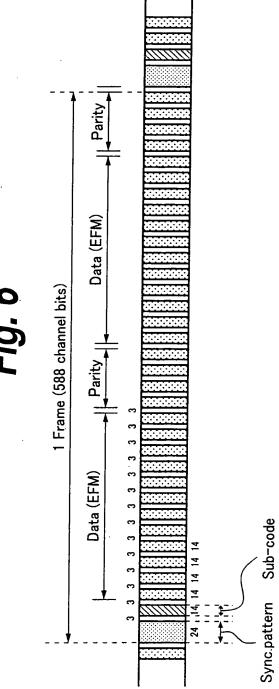


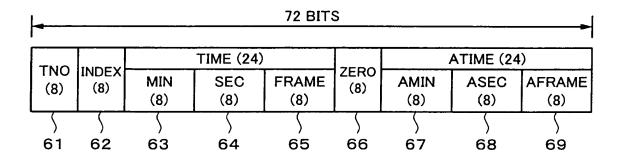
Fig. 6

Fig. 7

SYNCHRONOUS	CONTROL	ADDRESS	DATA\BITS	CRC
BITS	BITS	BITS		BITS
2 BITS	4 BITS	4 BITS	72 BITS	16 BITS

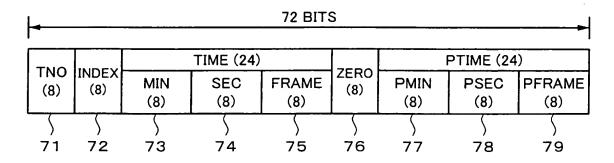
FORMAT OF Q CHANNEL

Fig. 8



FORMAT OF DATA BITS

Fig. 9



FORMAT OF DATA BITS

## Fig. 10A

MODE 1

SYNC (12 BYTES)

**HEADER (4 BYTES)** 

(2048 BYTES) **USER DATA** 

**AUXILIARY DATA** (288 BYTES)

## Fig. 10B

MODE 2

Fig. 10C

MODE 2 (FORM 1)

SYNC (12 BYTES)

SUB-HEADER (8 BYTES)

HEADER (4 BYTES)

**HEADER (4 BYTES)** 

SYNC (12 BYTES)

(2048 BYTES) **USER DATA** 

(2336 BYTES) **USER DATA** 

**AUXILIARY DATA** (280 BYTES)

## Fig. 10D

MODE 2 (FORM 2)

HEADER (4 BYTES) SYNC (12 BYTES)

SUB-HEADER (8 BYTES)

USER DATA (2324 BYTES)

EDC (4 BYTES)

Fig. 11A

<u> </u>			l
	W005		
MIN (8)	SEC (8)	FRAME (8)	MODE (8)

32 BITS

Fig. 11B

ADDRESS (24)	
24-BIT OR 23-BIT ADDRESS	MODE (8)

Fig. 12

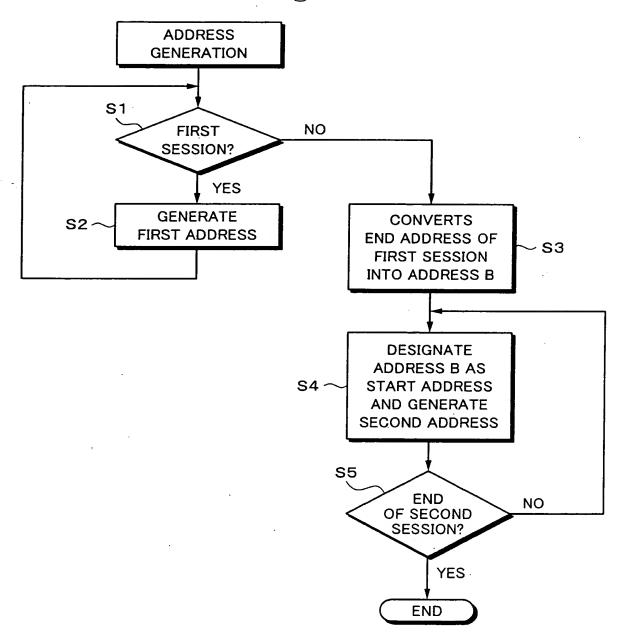


Fig. 13

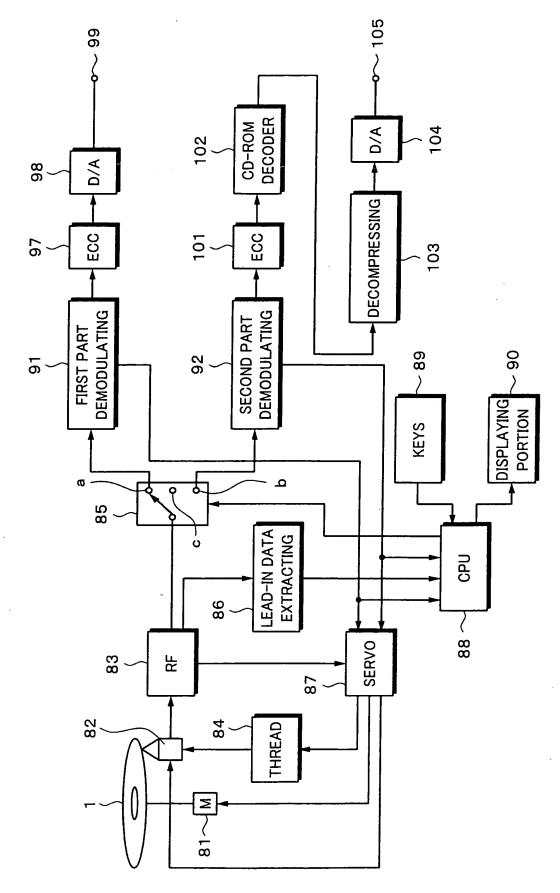


Fig. 14

